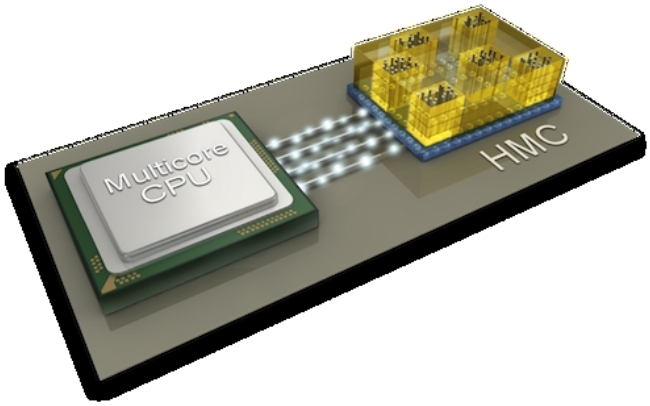
The Hybrid Memory Cube Consortium (HMCC) finishes the first specification for its titular memory technology-- HMC Specification 1.0, allowing OEMs to make 2 or 4GB DRAM employing a stacked, power-efficient architecture.



The result of a 17-month long collective effort led by Micron, Samsung and Hynix, the technology stacks multiple memory dies on top of a DRAM controller. In turn DRAM connects to the controller via silicon Vertical Interconnect Access (VIA), a technology passing a vertical electrical wire through a silicon wafer.

The structure reduces the tasks the memory chip performs, providing an interface 15x faster than standard DDR3 DRAM while reducing power requirements by -70% according to the HMCC.

In total the specification provides for chips with up to 160GBps of aggregate bi-directional bandwidth-- slightly faster than the current 11GBps of aggregate bandwidth of DDR3 or 18-20GBps of DDR4.

The consortium hopes to launch the first HMC products in H2 2013, before reaching consensus on the 2nd-generation specification (with output reaching 15-28GBps per pin) by Q1 2014.

"This milestone marks the tearing down of the memory wall," Micron comments. "The industry agreement is going to help drive the fastest possible adoption of HMC technology, resulting in what we believe will be radical improvements to computing systems and, ultimately, consumer applications."

HMCC members cover the globe and include the lines of Altera, ARM, Cray, Fujitsu, GLOBALFOUNDRIES, HP, IBM, Marvell, Micron Technology, National Instruments, Open-Silicon, Samsung, SK hynix, ST Microelectronics, Teradyne and Xilinx.

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